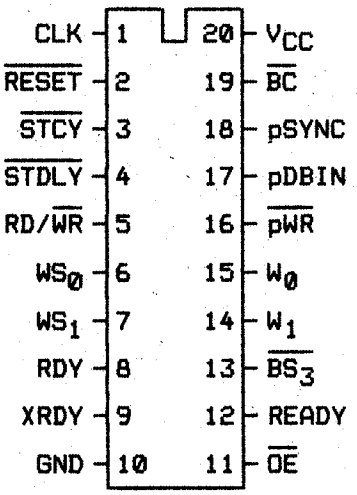
- **Performs bus cycle timing for IEEE-696 temporary masters**
- **Directly generates pSYNC, pDBIN and $\overline{\text{pWR}}$ strobes**
- **Programmable number of wait states in addition to external wait inputs**
- **Three-state outputs directly drive control bus**

16R801, 16R801A
TOP VIEW



description

The 16R801 provides all IEEE-696 bus timing signals for temporary masters, with the exception of pSTVAL*. The user must supply the pSTVAL* signal, as it relates to the status bus which is not generated by the 16R801. All bus cycle timing is derived from the CLK pin, which is usually the same signal as the bus clock. Bus cycles are started by bringing the $\overline{\text{STCY}}$ pin low, prior to the rising edge of CLK. An optional idle state may be inserted before the first pSYNC state by setting the $\overline{\text{STDLY}}$ pin low. A read or write cycle will be generated, depending on the level of the RD/$\overline{\text{WR}}$ input pin. Wait states are generated by either programming the WS_0 and WS_1 pins, or by bringing one of the ready pins RDY or XRDY low. If wait states are generated by both methods, the wait states requested by the RDY or XRDY pins are honored first.

pin description

CLK **Clock input.** All timing is referenced to the rising edge of this clock. In most applications, the CLK input is the same signal used to generate the bus ϕ signal.

$\overline{\text{RESET}}$ **Reset input.** Active low. Resets all outputs to their inactive levels on the next rising edge of CLK. $\overline{\text{RESET}}$ will override any cycle currently in progress.

$\overline{\text{STCY}}$ **Start cycle.** Active low. Starts a new bus cycle on the next rising edge of CLK. Sampled whenever no bus cycle is currently in progress, or during the last bus state of the current bus cycle. If $\overline{\text{STCY}}$ is inactive on the rising edge of the last bus state of a current cycle, the current cycle terminates and no new cycle is started.

$\overline{STDLY}$ **Start cycle delay.** Active low. Causes the first active bus state (pSYNC) to be delayed one clock if the new cycle was not immediately preceeded by another cycle. This mode is generally used the IEEE-696 DMA protocol is implemented at high speeds (above 5 MHz) where proper address and status set-up time may not be possible when a temporary master first takes control of the bus. This signal is not sampled when multiple bus cycles are performed consecutively.

RD/$\overline{WR}$ **Read / write control input.** Defines a read cycle if high or a write cycle if low. Must remain stable during bus state two (pDBIN or $\overline{pWR}$ active), but may change during the last bus state (BS_3).

WS_0, WS_1 **Wait state select inputs.** Up to three wait states may be programmed into the current cycle according to the chart below:

WS_1	WS_0	Number of wait states
0	0	None
0	1	1
1	0	2
1	1	3

Wait states programmed in this manner are inserted in addition to externally requested wait states. Externally requested wait states are honored first, followed by programmed wait states, if any. The WS_0 and WS_1 inputs must be stable before the start of bus state two.

RDY, XRDY **Ready inputs.** Active high. Both RDY and XRDY inputs must be high in order to complete a bus cycle. If either inputs are low when bus state two in entered, a wait state in inserted. Wait states will continue to be inserted as long as either ready input is low. Ready inputs are not sampled during programmed wait states.

READY **Ready output.** Active high. Synchronized version of the RDY and XRDY inputs.

$\overline{BS_3}$ **Bus state three output.** Active low. Goes active during the last bus state of the current cycle.

W_0, W_1 **Programmed wait state counter outputs.** Indicate the current down count of programmed wait states. Loaded after bus state one.

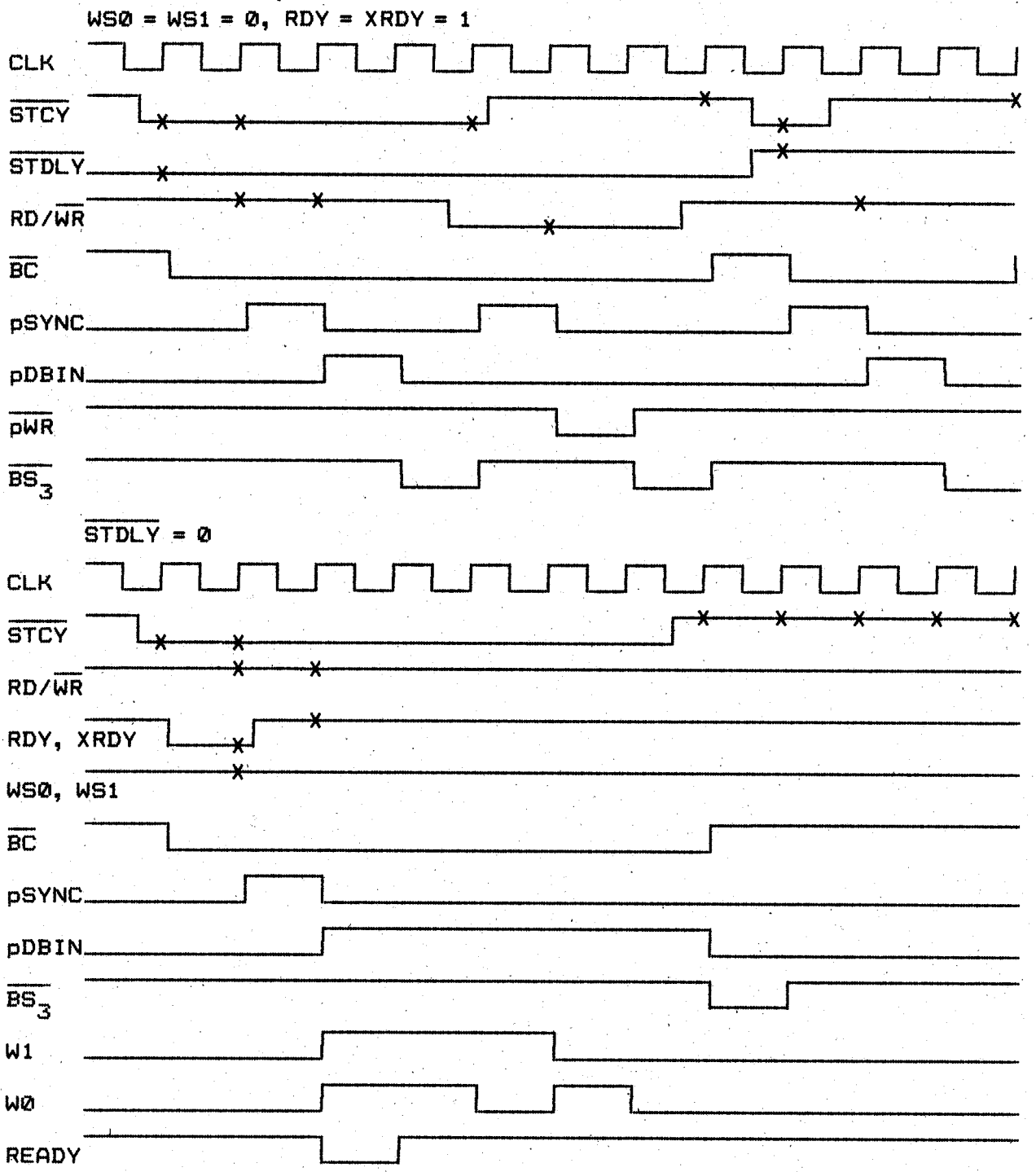
$\overline{pWR}$ **Write strobe.** Active low. Goes active for one clock period following pSYNC if RD/$\overline{WR}$ is low. May be extended an indefinite number of clock periods by inserting wait states. May be directly connected to the $\overline{pWR}$ bus signal if desired.

pDBIN **Read strobe.** Active high. Goes active for one clock period following pSYNC if RD/$\overline{WR}$ is high. May be extended an indefinite number of clock periods by inserting wait states. May be directly connected to the pDBIN bus signal if desired.

pSYNC **First bus state sync.** Active high. Goes active for one clock period at the beginning of each bus cycle. May be directly connected to the pSYNC bus signal if desired.

$\overline{BC}$ **Bus cycle output.** Active low when a bus cycle is in progress. Remains active as long as bus cycles continue. $\overline{BC}$ is inactive when no bus cycles are in progress. A high to low transition on this output indicates the start of a new bus cycle after an inactive period.

examples of state sequences



recommended operating conditions

PARAMETER	16R801 16R801A MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Low-level output current, I_{OL}			24	mA
High-level output current, I_{OH}			-3.2	mA
Operating free-air temperature	0		70	deg C

electrical characteristics over operating conditions

PARAMETER		TEST CONDITIONS		16R801 16R801A MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IK}	Input clamp voltage	V_{CC} = MIN I_I = -18mA			-0.9	-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX V_I = 0.4V			-20	-250	uA
I_{IH}	High-level input current	V_{CC} = MAX V_I = 2.4V				25	uA
I_I	Maximum input current	V_{CC} = MAX V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = MAX I_{OL} = MAX V_{IH} = MIN				0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = MAX I_{OH} = MAX V_{IH} = MIN		2.4	3.5		V
I_{OZ}	Off-state output current	V_{CC} = MIN V_{IL} = MAX I_{OH} = MAX V_{IH} = MIN	V_O = 0.4V V_O = 2.4V			-100 100	uA
I_{OS}	Short-circuit output current	V_{CC} = 5V		-30	-60	-90	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

switching characteristics over operating conditions

TEST CONDITIONS: R_1 = 200 ohms, R_2 = 390 ohms, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	16R801-1 MIN	TYP	MAX	16R801 MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}									ns
t_{PLH} t_{PHL}									ns
t_{PLH} t_{PHL}									ns
t_{PLH} t_{PHL}									ns