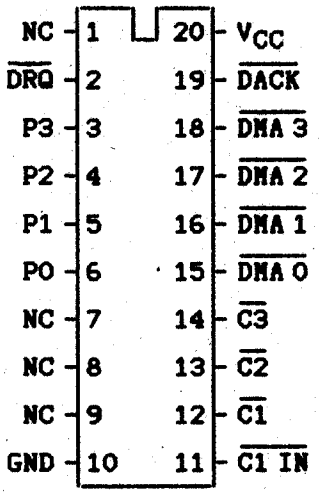
- Complete IEEE-696 DMA priority comparator in 20 pin package
- Open collector outputs directly drive DMA arbitration bus
- Fast parallel priority comparison

16L801A, 16HL01A-15
TOP VIEW



NOTE: Pin 12 must be externally connected to pin 11 for proper device operation.

description

The 16L801A contains the necessary logic to perform priority compares on the IEEE-696 DMA arbitration bus. Active high priority bits are presented at the P0 - P3 pins where P0 is the least significant bit. The input/open collector outputs $\overline{\text{DMA 0}}$ through $\overline{\text{DMA 3}}$ are connected to the DMA arbitration bus. When control of the bus is desired, the $\overline{\text{DRQ}}$ signal is brought low to place the priority present on the priority input pins onto the arbitration bus. If the logic levels on the DMA arbitration bus agree with the logic levels asserted by the 16L801A, the $\overline{\text{DACK}}$ output signal goes low indicating that the 16L801A is the highest priority requester. Any disagreements on the bus will cause removal of less significant bits and $\overline{\text{DACK}}$ to go high. Outputs $\overline{\text{C1}}$, $\overline{\text{C2}}$ and $\overline{\text{C3}}$ are intermediate product terms and are not intended to be useful output signals. The $\overline{\text{C1}}$ output must be externally connected to the $\overline{\text{C1 IN}}$ input for proper device operation.

function table

INPUTS					ARBITRATION BUS				OUTPUT
$\overline{\text{DRQ}}$	P3	P2	P1	P0	$\overline{\text{DMA 0}}$	$\overline{\text{DMA 1}}$	$\overline{\text{DMA 2}}$	$\overline{\text{DMA 3}}$	$\overline{\text{DACK}}$
H	X	X	X	X	X	X	X	X	H
L	L	L	L	L	L*	L*	L*	L*	H
L	L	L	L	L	H	H	H	H	L
L	L	L	L	H	L*	L*	L*	L	H
L	L	L	L	H	H	H	H	L	L
L	L	L	H	L	L*	L*	L	L*	H
L	L	L	H	L	H	H	L	H	L
L	L	H	L	L	L*	L	L*	L*	H
L	L	H	L	L	H	L	H	H	L
L	H	L	L	L	L	L*	L*	L*	H
L	H	L	L	L	L	H	H	H	L
L	H	H	H	H	L	L	L	L	L

L* indicates that one or more bits of the arbitration bus are being driven low by another requester and not by the 16L801A.

recommended operating conditions

PARAMETER	16L801A 16L801A-15 MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Off-state output voltage, $V_{O\ (off)}$			5.5	V
Low-level output current, I_{OL}			24	mA
High-level output current, I_{OH}			-3.2	mA
Operating free-air temperature	0		70	deg C

electrical characteristics over operating conditions

PARAMETER			TEST CONDITIONS	16L801A 16L801A-15 MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IK}	Input clamp voltage		V_{CC} = MIN I_I = -18mA		-0.9	-1.2	V
I_{IL}	Low-level input current	DRQ, Any P	V_{CC} = MAX V_I = 0.4V		-20	-250	uA
		Other inputs			-120	-350	
I_{IH}	High-level input current	DRQ, Any P	V_{CC} = MAX V_I = 2.4V			25	uA
		Other inputs				125	
I_I	Maximum input current		V_{CC} = MAX V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN V_{IL} = MAX I_{OL} = MAX V_{IH} = MIN			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN V_{IL} = MAX I_{OH} = MAX V_{IH} = MIN	2.4	3.5		V
I_{OS}	Short-circuit output current		V_{CC} = 5V	-30	-60	-90	mA
I_{CC}	Supply current		V_{CC} = MAX		110	155	mA

switching characteristics over operating conditions

TEST CONDITIONS: R_1 = 200 ohms, R_2 = 390 ohms, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	16L801A-15 MIN	TYP	MAX	16L801A MIN	TYP	MAX	UNIT
t_{PLH}	DRQ, $\overline{CI}$ IN	DACK			15		12	25	ns
t_{PHL}					15		12	25	
t_{PLH}	DRQ, $\overline{CI}$ IN	Any $\overline{DMA}$			15		12	25	ns
t_{PHL}					15		12	25	
t_{PLH}	Any P, Any $\overline{DMA}$	DACK			30		24	50	ns
t_{PHL}					30		24	50	
t_{PLH}	Any P, Any $\overline{DMA}$	Any $\overline{DMA}$			30		24	50	ns
t_{PHL}					30		24	50	